Please amend the present application as follows:

Specification

The following is a marked-up version of the specification with the language that is underlined ("___") being added and the language that contains strikethrough ("—" or double square brackets "[[]]" if the strikethrough is not easily perceivable, *i.e.*, "4" or a punctuation mark) being deleted:

Please amend the paragraph starting on p. 2, line 23 as follows:

To prevent ESD from damaging semiconductor circuits, various protective schemes may be employed. Large-scale protective schemes are often used to protect system level equipment. Examples of these schemes include, but are not limited to, the following: electrical grounding of technicians via wrist bands; the prevention of electrostatic build-up through the use of static-safe clothing, static control shoes, and high humidification; and the use of specialized shipping containers and storage bags. All of the above methods help to prevent the build-up of static charge. Additionally, small-scale, chip specific[[,]] approaches may be used. Often, high-current clamping devices are placed on the pins of a chip so that the high currents associated with an ESD event are safely shunted without away from the circuitry.

Please amend the paragraph starting on p. 5, line 5 as follows:

The circuit of Figure 1 operates in the following manner. When a large negative voltage is present at pad ~~100~~ 118, the forward junction from base 208 to emitter 204 is turned on, creating, in effect, a short circuit between base 208 and emitter 204. Thus, the negative charge is delivered to ground 210 instead of traveling to the circuit being protected at 114.

Please amend the paragraph starting on p. 5, line 10 as follows:

When a large positive voltage is present at pad ~~100~~ 118, there is a large voltage between emitter 204 and base 208, resulting in a "soft" breakdown of the *pn* junction. Preferably, this breakdown occurs at a voltage higher than the operating voltage of the circuit to be protected. The transistor is then operating in the inverse or reverse ode. Collector 206 acts as an emitter and emitter 204 acts as a collector. However, the gain, β, of this transistor in the reverse mode is low, about 4 or 5, as opposed to a β of about 100 for a transistor connected in the typical

configuration. The junction between the emitter and the base becomes forward biased; *i.e.*, the transistor is in reverse operation mode. The current is shunted through collector 206 when the base voltage is greater than the collector voltage by about 0.7 volts. Thus, the current caused by the high voltage present at the input is shunted through emitter 204 to collector 206 to ground. Resistor 212 acts to cause a voltage drop between ground 210 and base 208. Resistor 212 may not be necessary if the intrinsic resistance of transistor 202 is sufficiently large to maintain an appropriate base voltage greater than the voltage at collector 206.